Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1-28.   (Canceled)

29.   (Currently Amended) A method of executing a sequence of instructions comprising:

comparing a subset of bits from a first operand to a subset of bits from a

second operand to determine determining a predicted predicate value (PPV) for a

predicate of a predicated instruction, the PPV having a value of TRUE or FALSE;

conditionally executing the predicated instruction, if the PPV has a value of

TRUE;

executing a COMPARE instruction to determine an actual predicate value

(APV) for the predicate of the predicated instruction;

comparing the APV to the PPV; and

flushing a pipeline if the APV and the PPV are unequal.

30.   (Previously Presented) The method of claim 29, further comprising executing the

predicated instruction after flushing the pipeline.)

31.   (Previously Presented) The method of claim 29, wherein flushing the pipeline

comprises flushing only a backend portion of the pipeline.

32.   (Previously Presented) The method of claim 29, further comprising updating

historical information corresponding to the predicate of the predicated instruction in a

predicate history table after comparing the APV to the PPV.

33.   (Canceled)

34.   (Previously Presented) The method of claim 29, wherein conditionally executing the

predicated instruction includes treating the predicated instruction like a no-op if the value of

the PPV is FALSE.

35.   (Currently Amended) A processor comprising:

        a predicate history table;

        a register file; and

        a predicted predicate value (PPV) calculator having a first input coupled to an

output of the predicate history table and a second input coupled to an output of the

register file, the PPV calculator to calculate a PPV by comparing a subset of bits from

a first operand to a subset of bits from a second operand, having a value of TRUE or

FALSE, for a predicated instruction.

36.   (Previously Presented) The processor of claim 35, further comprising:

a IP select circuit having an output coupled to the predicate history table;

a register select circuit having an output coupled to the register file; and

an instruction decoder having an output coupled to input of the IP select

circuit and the register select circuit.

37.   (Previously Presented) The processor of claim 35, further comprising a pipeline

having a PPV input coupled to an output of the register file and an actual predicate value

(APV) output coupled to an input of the predicate history table.

38.   (Previously Presented The processor of claim 37, further comprising an XOR gate

having a first input coupled to the APV output of the pipeline, a second input coupled to an

output of the register file, and an output coupled to a flush input of the pipeline.

39.   (Currently Amended) A processor comprising:

a predicate history table to store historical information associated with a predicate of

a predicated instruction; and

a predicted predicate value (PPV) calculator to calculate a PPV for the predicated

instruction by comparing a subset of bits from a first operand to a subset of bits from a

second operand, the PPV having a value of TRUE or FALSE.

40.   (Previously Presented) The processor of claim 39, further comprising a speculative

predicate register file to store the PPV.

41. (Previously Presented) The processor of claim 40, further comprising a pipeline to receive the PPV, and to conditionally execute the predicated instruction if the PPV has a value of TRUE.

42. (Previously Presented) The processor of claim 39, further comprising a pipeline to receive the PPV, and to conditionally execute the predicated instruction if the PPV has a value of TRUE.

43. (Canceled)

44. (Previously Presented) The processor of claim 39, wherein the calculator includes a selector to, based on a confidence level, select the PPV to be based on historical information.

45. (Currently Amended) A system comprising:

     memory to store a predicated instruction;

     a bus to transfer the predicated instruction from the memory; and

     a processor to receive the predicated instruction and to calculate a predicted predicate value (PPV) for the predicate of the predicated instruction by comparing a subset of bits from a first operand to a subset of bits from a second operand, the PPV having a value of TRUE or FALSE.

46. (Previously Presented) The system of claim 45, wherein the processor comprises a predicate history table to store historical information associated with the predicate of the predicated instruction.

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47.   (Previously Presented) The system of claim 46, wherein the processor further comprises a pipeline to receive the PPV, and to conditionally execute the predicated instruction if the PPV has a value of TRUE .

48.   (Previously Presented) The system of claim 45, wherein the processor further comprises a pipeline to receive the PPV, and to conditionally execute the predicated instruction if the PPV has a value of TRUE.

49.   (Previously Presented) The system of claim 45, wherein the memory is main memory and the bus is a system bus.

50.   (Previously Presented) The system of claim 45, wherein the memory is external memory.